On-chip Integrated Antenna Structures in CMOS for 60 GHz WPAN Systems

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Abstract—We present several on-chip antenna structures that may be fabricated with standard CMOS technology for use at millimeter wave frequencies. On-chip antennas for wireless personal area networks (WPANs) promise to reduce interconnection losses and greatly reduce wireless transceiver costs, while providing unprecedented flexibility for device manufacturers. We present the current state of research in on-chip integrated antennas, highlight several pitfalls and challenges for on-chip design, modeling, and measurement, and propose several antenna structures that derive from the microwave and RF communication fields. We also describe an experimental test apparatus for performing measurements on RFIC systems with on-chip antennas at The University of Texas at Austin.

Index Terms—WPAN, 60 GHz, RFIC, on-chip antenna, millimeter wave, mmWave communications, passive radiating elements.

I. INTRODUCTION

Within the past decade, the wireless community has become increasingly interested in the worldwide 60 Gigahertz (GHz) radio frequency (RF) band [1–8]. In 2001, the United States Federal Communications Commission (FCC) released 7 GHz of bandwidth (57-64 GHz) for unlicensed use, while other governments have similarly allowed portions of the 60 GHz band to be used without a license. While the precise frequency allocation is different in each country, all bands share a common 5 GHz of continuous unlicensed bandwidth centered at 60 GHz [5, 6].

With such large RF bandwidths available at 60 GHz, data rates of several gigabits per second (Gbps) are feasible within local areas, greatly surpassing current wireless transmission capabilities. Wireless personal area networks (WPANs) at 60 GHz will enable a vast array of applications such as wireless memory and uncompressed high definition video. However, for 60 GHz technology to be adopted rapidly, device and system costs and power consumption must be kept as small as possible. Fully integrated CMOS circuitry offers the greatest cost and power savings, especially when considering packaging, integration, and interconnect issues. Already there has been significant work in RF circuits and systems operating at 60 GHz using CMOS technology [9–16].

A key factor for the implementation of low cost 60 GHz systems is integrating an antenna on-chip with CMOS circuits so that an entire wireless communication system can be manufactured in one step with foundry fabrication. Even if only passive antennas are fabricated on a chip, easy integration with other circuitry on a form factor such as a printed circuit board (PCB) is possible with no power drain by the antennas. Essentially, on-chip antennas, whether passive or active with basic RF amplification stages, would provide many degrees of freedom for the design and implementation of consumer electronic devices, while eliminating or greatly reducing material costs associated with RF antennas. The large antenna gains and pattern flexibility at 60 GHz will support reliable low power, high bandwidth communications over short distances with minimal power drain, as the antenna gains are traded for transmitted power consumption to overcome RF propagation losses and obstructions in the channel [5, 7, 8]. Integrating antennas with RF circuitry has been pioneered in [17, 18], and several papers have documented work fabricating standalone integrated circuits at 60 GHz [9–11].

Combining RF circuits with integrated antennas at 60 GHz poses several major challenges. Standard CMOS technology is not optimized for millimeter wave structures, and losses in the IC metal layers and substrate greatly reduce antenna performance. Another challenge is the small distance (typically several microns) between the radiating elements, the surrounding metal layers, and low-resistance silicon that exists underneath the metal layers of the IC substrate, which act to distort the normal radiation patterns that antenna engineers are accustomed to in free space. Also, accurate high frequency modeling of devices and passive components at millimeter wave frequencies is difficult and accurate measurement of 3-D far field patterns for integrated antennas at 60 GHz has yet to be achieved.

Section II presents several novel on-chip antenna concepts, with extensive modeling and simulation results. These antenna concepts indicate promising approaches for on-chip antennas. Section III describes an experimental measurement system being developed at The University of Texas at Austin for testing and measuring on-chip antenna radiation patterns and wireless communication systems up to 67 GHz. The paper concludes with a synopsis of open research issues.
II. NEW CONCEPTS FOR 60 GHz INTEGRATED ANTENNAS

For on-chip antennas, interactions with the ground plane and the lossy silicon substrate causes near field energy to dissipate rapidly around the antenna, which greatly reduces radiation efficiency and gain. Researchers and amateur (ham) radio operators have long known of the issues of transmitting over ground planes and the benefits of phasing and switching with passive high gain antennas. Antenna gain towards the horizon has usually been the figure of merit for hams. They have communicated over great distances throughout the world by stacking and phasing these directional antennas in an array. It is conceivable to create high gain antennas at millimeter-wave frequencies on ICs by properly scaling antenna dimensions. High gain antennas such as the rhombic [19], the Yagi, the long wire [20], and even low-profile [21] and loop antennas [22] have been commonly used throughout history, and are now considered for the novel application of passive integrated millimeter wave antennas. This section considers the design of popular HF antennas for use at millimeter wave frequencies on a CMOS substrate.

A. Overview of Simulation Methods

We considered a substrate model for standard CMOS 0.18μm IC technology as shown in Figure 1. We model a chip with common dimensions of 5 mm x 5 mm with 6 metal layers above bulk silicon. Since the modeled ground plane is confined to the dimensions of the chip, diffraction may introduce radiation on the lower hemisphere (below the die). The dielectric between metal layers (silicon dioxide) is modeled as lossless, while the losses in silicon bulk substrate are modeled with conductivity (σ) of 10 S/m, as in [23] and in [24]. All simulations use a standard 50 Ω source impedance in series with the excitation.

![Fig. 1. Illustration of IC model including silicon dioxide layers for a typical CMOS integrated circuit.](image)

Realistic millimeter wave antennas were modeled with Ansoft HFSS (High Frequency Structural Simulator), a leading commercial finite element method field solver which simulates three-dimensional structures and produces S-parameters and radiation patterns. HFSS is used in both [25] and [26], as well as numerous other works.

The effective wavelength at 60 GHz for an IC substrate is estimated by using the frequency and material properties of the top IC layer (silicon dioxide, εᵣ = 3.9), where

\[ \lambda_{\text{freespace}} = \frac{1}{\sqrt{\varepsilon_0 \mu_0 f}} \]  
\[ \lambda_{\text{effective}} = \frac{1}{\sqrt{\varepsilon_\text{eff} \mu_0 f}} = \frac{\lambda_{\text{freespace}}}{\sqrt{\varepsilon_\text{eff}}} \]  

where \( \lambda_{\text{freespace}} \) is 5 mm for 60 GHz, and \( \lambda_{\text{effective}} \) is calculated by including the effect of the dielectric constant. Thus, \( \lambda_{\text{effective}} = 2.53 \) mm.

We explored on-chip antennas based on the basic half­wave dipole, the multi-element Yagi, and the rhombic antenna. These simple antennas have historically been very reliable and provide reasonable gain, high front-to-back and front-to-side ratios, and radiation near the horizon.

We identified the following key issues: a) how performance is a function of on-chip placement of radiating elements; b) how design guidelines should be applied to on-chip antenna design; c) the tolerances that exist between the widths, lengths, and spacings for various radiating and parasitic elements; and d) the maximum and direction of achievable gain for a wide range of new integrated passive on-chip antennas.

B. Feed Systems

In order to accurately simulate antennas, the transmission lines and feed systems that carry the signal from the on-chip transmitter outputs to the antenna inputs must be considered. Two feed systems were examined in simulation and yielded very comparable results. The feedlines extended from Metal 6 down to Metal 1, to transfer the signal from a lower layer to the top layer, as shown in Figure 1. Two representative feedlines are shown in Figures 2 and 3.

![Fig. 2. Feed system for dipole antenna.](image)

C. On-chip Dipole Antenna at 60 GHz

To understand on-chip antenna properties, we first considered half wave dipoles using a wide range of line widths and orientations. The best performance with respect to gain was obtained by placing a center fed dipole on the edge of the chip (See Figure 4).
Using equation (2), an on-chip dipole with length $\lambda/4 = 632.5 \mu m$ was simulated using a $30 \mu m$ antenna width. Each dipole $\lambda/4$ element was shortened to $570 \mu m$ to shift minimum $S_{11}$ up to 60 GHz as seen in Figure 5. When the width of the dipole elements is doubled to $60 \mu m$ while keeping the lengths the same, we observed that $S_{11}$ is minimized at 56.5 GHz (as opposed to 59.5 GHz). If the dipole is mounted on the center of the chip, as opposed to the edge, then the gain is a very poor -13.6 dBi, due to the lossy substrate and the close proximity of the radiation angle to the horizon. As shown in Figure 4, the edge mounted antenna (width of $30 \mu m$) exhibits maximum gain of -7.3 dBi at an elevation angle of $0^\circ$ above the substrate horizon ($\theta = 90^\circ$), and has a typical broadside pattern. This directionality provides the on-chip circuitry some radiation protection. Radiation efficiency is still poor, at approximately 9%. With element widths of $60 \mu m$, the maximum gain increases to -6.7 dBi, approximately 9 dB less than that of a free space dipole antenna. These significant changes highlight the importance of understanding on-chip antenna performance as it is relatively unknown today.

D. On-chip Yagi Antenna at 60 GHz

The Yagi antenna uses parasitic metals around the dipole to reflect and direct energy to achieve increased gain. There are several degrees of freedom when designing a Yagi antenna, such as the spacing, lengths, and widths of each parasitic element. We examined how spacing and widths affect Yagi performance on silicon, as well as the optimal antenna orientation to achieve maximum gain.

Simulations of a 2-element Yagi, consisting of a driven element and a parasitic reflector, showed highest gain when a Yagi antenna was cornered along the chip edge as shown in Figure 6. Using a thinner dipole width $w = 15 \mu m$, the Yagi dipole (driven element) length was adjusted to maintain a minimum $S_{11}$ at approximately 60 GHz. Optimal performance was found when each leg of the driven element was increased to $\ell = 597 \mu m$ (approximately 5% longer than the single dipole). The center feed spacing between each $\lambda/4$ element was $7 \mu m$. 

Fig. 3. Feedline of Yagi antenna.

Fig. 4. Top view of on-chip integrated dipole antenna (not to scale) and radiation pattern for this antenna. Maximum gain is -7.3 dBi (radial power units are in dBi). $\theta$ is the elevation angle where the Z-axis is $0^\circ$, and the XY plane is $90^\circ$. $\phi$ is the azimuthal angle in the XY plane, where the X-axis is $0^\circ$ and the Y-axis is $90^\circ$.

Fig. 5. $S_{11}$ characteristics of two dipole antennas with different element widths.

Fig. 6. Top view of three individually simulated two-element on-chip Yagi antennas (not to scale). The Yagi antenna was simulated at the center, lower right corner, and right edge of the 3mm x 5mm chip.
We first investigated performance as a function of the distance between the reflector and the driven element of a Yagi antenna. The Yagi dipole was placed at the center of the 5mm x 5mm chip. According to [22], Yagi reflectors in free space should be spaced between 0.15\(\lambda\) and 0.20\(\lambda\). Given that the Yagi quarter-wave driven element resonated at \(\ell = 597\ \mu m\), we estimated the wavelength to be 2.388 mm, which is comparable (within 4\%) to our result from (2), and denoted this length as \(\lambda\). A reflector was iteratively positioned from 0.01\(\lambda\) to 0.25\(\lambda\) in increments of 0.01\(\lambda\) away from the dipole. We observed S11 and gain. The reflector width \(w_y\) was identical to the dipole (15 \(\mu m\)) and the length was set to \(\ell_y = 0.55\lambda\), as suggested by [22]. Figure 7 shows a comparison of S11 of the Yagi antenna as the reflector was moved away from the dipole. Note the S11 resonance is shifted to a lower frequency when a reflector is added and the minimum S11 occurred when the Yagi reflector was 0.11\(\lambda\) away from the dipole. To bring the resonance back up to 60 GHz using a 0.11\(\lambda\) spaced reflector, each driven element was scaled to 574 \(\mu m\) in order to resonate at the appropriate frequency, denoted in Figure 7. Gains increase slightly with the addition of the reflector, which is consistent with antenna theory. Gains increased as the reflector was moved away from the dipole. At spacings between 0.20\(\lambda\) and 0.25\(\lambda\), the maximum gains were very similar, with a reflector distance of 0.25\(\lambda\) having the highest gain at the horizon, shown in Figure 8. At distances larger than 0.25\(\lambda\), gain was further diminished. Thus, it appears Yagi antennas with a 0.25\(\lambda\) reflector spacing exhibit both a reasonable S11 to a 50\(\Omega\) source impedance and maximum horizon gain.

With a 0.25\(\lambda\) spacing, we investigated the role of reflector width in Yagi performance. The spacing was held constant at 0.25\(\lambda\) from the edge of the driven element to the edge of the reflector. S11 decreased slightly by 1 dB overall as the reflector width was increased from 15 \(\mu m\) to 160 \(\mu m\). We noted incremental gain increases as width was increased, differing only by 0.5 dB over the entire range of widths. This shows that the width of the reflector conductor does not appreciably impact gain or impedance matching of the on-chip Yagi. As we will show subsequently, this does not hold true for rhombic antennas.

Finally, we investigated how Yagi performance changes as the antenna is moved across the chip. We used the 0.25\(\lambda\) spaced reflector with width 160 \(\mu m\). We placed the antenna at the center, right edge, and lower right corner of the chip as seen in Figure 6. Figures 9 and 10 show the S11 and gain changes as the antenna is moved, respectively. The performance is compared to that of a dipole at the center of the chip. The 2-element Yagi along the right corner of the chip achieved the highest gain of -3.55 dBi, a front-to-back ratio of 10.4 dB, and maximum radiated intensity at 20 ° above the horizon. The efficiency was 15.8\%, which is much greater than the numbers...
reported in [23, 25, 26]. By moving the Yagi antenna to an edge, maximum gains improved by 7.65 dB compared to the Yagi located at the center of the chip and by 10.05 dB over a dipole at the center of the chip.

E. On-chip Rhombic Antenna at 60 GHz

The rhombic antenna is a diamond shaped broadband directional antenna commonly used in the 3 - 30 MHz frequency range by shortwave broadcast stations and ham radio operators. Large rhombic structures are constructed several meters above ground. Here we consider scaling them to on-chip solutions. To implement a true rhombic antenna, each leg of the antenna must be longer than two wavelengths [27]. This poses a problem for on-chip antenna designers: if \( \lambda \) in the material is approximately 2.5 mm, we are barely able to fit a leg of length 2\( \lambda \) on the edge of our 5 mm chip, although larger chips could easily be fabricated for more directive passive antennas.

We considered a rhombic antenna along the perimeter of the chip where each leg length is approximately 4.9 mm (nearly 2\( \lambda \)) as shown in Figure 11. The rhombic antenna was fed with a 60 GHz source and a 50 \( \Omega \) source impedance. Two primary design parameters of a rhombic antenna in free space are the angle \( \gamma \) (indicated in Figure 11) and the height above ground. The ground height is analogous to the substrate thickness of the chip and can be optimized using wafer thinning techniques. A third rhombic design parameter, exclusive to small scale antennas such as an on-chip antenna, is trace width (indicated in Figure 11). These three design parameters were varied to ascertain the performance of on-chip rhombic antennas operating at 60 GHz.

![Fig. 11. Top view of a simulated 60 GHz on-chip rhombic antenna. The rhombic angle \( \gamma \) and trace width are indicated. The point where the antenna is connected to the 60 GHz source is denoted "Feed Points."](image)

The first design parameter tested was the rhombic angle, \( \gamma \). The substrate thickness was held constant at 750 \( \mu m \), feed points were separated by 3 \( \mu m \), and trace width was 10 \( \mu m \). The angle \( \gamma \) was incremented from 5° to 45°. Antenna gain at the horizon (\( \phi = 90°, \theta = 90° \)) as well as maximum gain were observed. The results in Figure 12(a) show that the angle of largest horizon gain is \( \gamma = 39° \).

Using \( \gamma = 39° \), the substrate thickness was decreased from 750 \( \mu m \) to 50 \( \mu m \). The results shown in Figure 12(b) demonstrate that horizon gain increases as the substrate thickness is decreased. An optimal value for horizon gain is observed at 110 \( \mu m \) or approximately \( \lambda/25 \). A thinner substrate allows higher gains and efficiencies since the degrading effects of the lossy silicon substrate are reduced.

Using both a 39° rhombic angle, and a 110 \( \mu m \) substrate thickness, the trace width of the on-chip rhombic was in-
creased from 10 μm to 1900 μm. The results are shown in Figure 12(c). The maximum horizon gain occurs with a trace width of 1445 μm (about 57%λ) with a gain nearly -3 dBi. The angle of maximum gain begins to shift from the horizon as trace width increases.

Generally, free space rhombic antennas are constructed of electrically thin copper wires, so the thickness of these wires is not a design parameter. However, repeated tests have shown that on-chip rhombic antenna performance is enhanced with thicker trace widths. Figure 13 shows a comparison between a conventional rhombic antenna with thin trace widths and a higher gain rhombic antenna with thicker trace widths. Azimuth and elevation radiation plots are presented in Figure 13. The rhombic antenna with trace width 200 μm achieves a horizon gain of -8 dBi while the rhombic with trace width = 1445 μm can achieve a greater horizon gain close to 0 dBi.

The rhombic antenna has been optimized with respect to horizon gains; however, to transfer maximum power to the antenna, the S11 should be minimized at 60 GHz. If a matching network is not available to minimize S11, the width of the feed points can be adjusted. The rhombic feed width was adjusted to 660 μm (26% of λ) to obtain an acceptable impedance match to the standard 50 Ω source impedance. This caused the S11 to decrease to a flat -13 dB and thus allow most of the available power to be accepted by the antenna when transmitting. Additionally, the horizon gain of the antenna slightly increased from -3 dBi to -1.27 dBi with the increased feed width. The S11 of -13 dB for the on-chip rhombic antenna was flat across the entire 57-64 GHz band which shows wide bandwidth.

The optimized rhombic antenna with radiation pattern is shown in Figure 13. Horizon gain was -1.27 dBi and overall maximum gain was -0.2 dBi. The radiation efficiency was 85%, due primarily to a thinned lossy substrate. These gains occurred with γ = 39°, 110 μm substrate thickness, 1445 μm trace width, and a feed width of 660 μm.

Although the simulation results are promising for the rhombic, the size of the antenna and the area used by it on the chip may cause electromagnetic interference with circuit components, thus suggesting several rhombics may best be packaged as a standalone passive chip.

III. FACILITIES FOR ON-CHIP ANTENNA WORK AT THE UNIVERSITY OF TEXAS AT AUSTIN

The Wireless Networking and Communications Group (WNCG) at The University of Texas has invested approximately $1,000,000 to build a start-of-the-art measurement facility for RF circuitry and on-chip antennas up to 67 GHz (see Figure 14). The facility includes a probe station consisting of several devices for making in-situ measurements on circuit substrates, and allows for thorough characterization of all S-Parameters (e.g. VSWR, gain, coupling losses), as well as other related equipment operating up to 67 GHz.

By using the probe station and vector network analyzer, it is possible to create a 3-D antenna pattern range. We have calculated the minimum far-field distance of the on-chip antenna, given by [28], to be only 10 mm.

![Fig. 13. Comparison of two 60 GHz on-chip rhombic antennas. Increasing trace widths increases horizon gains, as seen in the radiation plots (φ = 90°, θ = 90°, radial units in dBi). The wide rhombic antenna showed gains increased by 6-8 dBi when trace widths were increased from 200 μm to 1445 μm.](image)

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![Fig. 14. Measurement facilities in the WNCG lab at UT Austin](image)

In order to confirm fabricated on-chip antennas, we are...
constructing an automated antenna measurement system that makes use of a rotating conical horn antenna. The system in Figure 15 is based on the system described in [29]. In our system, the receiving antenna rotates on an axis at a constant distance from the probe-fed IC antenna, acquiring field measurements for one cut of the radiation pattern (where the ϕ (azimuth) angle is fixed, while the θ (elevation) is incrementally stepped). This rotation is automated by a computer-controlled motor that accurately records position data while received power is measured. When one rotational “cut” is completed, the base of the rotation is moved as indicated along the plate edge, changing the ϕ angle and repeating the θ angle sweep. This system allows us to construct a far field radiation pattern for a large range of elevation and azimuth angles.

It is crucial that all reflective surfaces and other possible interferers, especially the probe station, be covered with radio-absorbing material. Pre-test and calibration will account for losses from cables, probe tips, and other elements in the measurement system. Wideband channel sounding methods may be used here.

IV. CONCLUSION

We have presented various 60 GHz passive antennas simulated for implementation on an integrated circuit. Typical CMOS metals, dielectrics, and substrates were used. Antennas were designed to fit on an IC die size of 5mm x 5mm. The antennas implemented were the dipole, Yagi, and rhombic antennas. We found key relationships between the dipole and the Yagi elements spacing and found antenna performance is maximized when the antennas are placed at the edge of the die. Based on S11, the Yagi antenna resonated best with a 0.11λ reflector spacing. When moving from the center of the chip to the right edge, the maximum gains of both the dipole and Yagi antenna increased by nearly 7 dB. At the corner of the chip, the dipole and the 2-element Yagi had maximum gains of -6.7 dBi and -3.5 dBi, respectively.

A novel application of the rhombic antenna to IC technology is also explored. Here, we find the optimal angle, substrate thickness and trace width for implementing rhombic antennas in CMOS technology. Using these optimal parameters, simulations show that it is possible to achieve an antenna gain of -0.2 dBi, the highest reported for any on-chip antenna.

While our results show higher gains than previously reported, on-chip antennas tend to have very low efficiencies and pose a unique challenge for antenna designers. However, integrating antennas with circuitry will greatly advance communications technology by improving performance and lowering costs for WPAN systems.

REFERENCES