I. 60GHZ WIRELESS SYSTEMS ADVANTAGES AND CHALLENGES

The 60GHz band has recently been allocated worldwide for unlicensed wireless communications systems. The US, Europe and Japan have all allocated at least 5GHz of contiguous bandwidth, which is nearly equal to all other wireless communications, combined. This unprecedented amount of bandwidth holds the potential for much higher data rates than other channels that are bandwidth-limited. Wireless data rates in the range of 1Gbps become reasonable.[3] [6]

There are some major disadvantages to the 60GHz band. Probably the most important aspect of the 60GHz band for low-power wireless communications is the path loss. Path loss will be discussed in more depth below, but it suffices to say that an omnidirectional antenna at 60GHz suffers from severe path loss. Another difficulty in using the 60GHz band is that circuits are more difficult to design and implement, as compared to the lower-frequency bands in widespread use today. In the interest of higher system integration and therefore lower system cost and power consumption, we would like to implement all the circuits in standard CMOS, in this case 130nm. This also compounds the problem of implementing the circuits. The f_{MAX} of NMOS devices in 130nm CMOS is approximately 130GHz, which means that under optimal conditions a single-stage amplifier can be expected to achieve no more than 4-6dB of gain at 60GHz.[5] CMOS has the advantage that it can support very large amounts of digital processing in a very small area and for very low power. The key to building advanced communications systems in CMOS, especially at a 60GHz carrier frequency, is to leverage the digital computational power of CMOS.

II. THE CASE FOR AN ADAPTIVE ANTENNA ARRAY

In shifting to the higher 60GHz carrier frequency we are also reducing the wavelength of the carrier signal, which has a marked effect on the antenna system that is required. If a nominally omnidirectional antenna is used the path loss will scale inversely with the square of the wavelength. Path loss can be calculated as: [1]

$$PL = \left(\frac{\lambda}{4\pi R}\right)^2$$

This means that the extra path loss incurred in moving from 5GHz to 60GHz is 22dB, for a grand total of 88dB of path loss at 10m for an omnidirectional antenna at a 60GHz carrier frequency. Furthermore, it is reasonable to assume that the transmit power of a 60GHz communications system will be roughly equal to its cousins operating at lower frequencies. However, due to the limitations of CMOS circuits, it will be more difficult to achieve that power. Under these two assumptions it quickly becomes apparent that in order for a 60GHz system to operate at high data rates at a reasonable range the path loss must be recouped. Other than simply increasing the transmit power of the system, which may not be an option at all, the only way to overcome this loss is by using a high-gain antenna.

The only practical way to achieve high antenna gain in a changing or mobile environment is to use an adaptive antenna array [1]. The key is that this class of antennas can achieve high gain in a nearly arbitrary direction. The direction of the main beam can be adapted electronically on-the-fly to achieve the optimal antenna gain at any moment.

The number of antennas for the system should be chosen to combat the path loss incurred by the system, and even further improve the signal to aid the rest of the system. For rather arbitrary system specifications of 1Gbps at 10 meters, with some safety margin, we can see that approximately 16 antennas will be needed on the transmit and receive sides. [6]

III. SUBDIVISION OF THE POWER AMPLIFIER

In utilizing an array of antennas we reap the benefit of increased antenna directivity. However, there is another very important benefit. Now that there are N separate signals driving N separate antennas, there can be N separate power amplifiers, or PA's. Each PA drives its own antenna, and the power from the array is combined in space as described above. Therefore the total transmit power of the system is the sum of the power output of all the PA's. The power output requirement for each individual PA is then reduced to 1/N of the total required for the system. This reduction in performance is critical for future CMOS designs where supply voltages are near or even below 1 V.

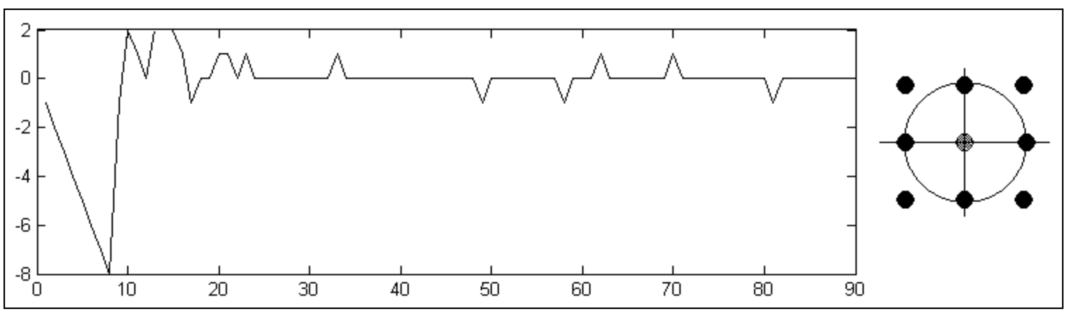

Figure 1. Angle error due to quantization of antenna weights

When adding antennas to the transmitter we obtain a double win for each antenna added. For each added antenna the directivity is increased by one, but the total transmit power is increased by one unit as well, if we add a duplicate PA for each new antenna. Therefore, if we add a duplicate PA for each new antenna the Effective Isotropic Radiated Power (EIRP) is quadrupled for each doubling in the number of antennas. This means that a system that uses 16 antennas for the transmitter and 16 antennas for the receiver will have a gain of (16+16+16) = 36dB over a system with a single antenna and PA.

IV. PHASE SELECTION ACCURACY

In designing the RF front-end for a beamforming system an important consideration is the accuracy requirement of the phase shift for each antenna. Recall that the phase shifts are relative, and so systematic errors in the phase of any individual antenna can be removed, as will be discussed later. The phases of the array should be controlled digitally, and that means that the phase shifts will be quantized. [2] Simulations were carried out to test the accuracy requirements. A beam was swept from 0 to 90 degrees, and at each point the beam with floating-point weighting coefficients was compared to a beam formed by quantizing the weighting coefficients.[6] The angle of the main beam was determined for the quantized case, and this was compared to the ideal case, with the error plotted in Figure 1.

It is also important to note that a phase shift that is common to the signals of all the antennas will not produce a change in the beam or antenna pattern. This includes the modulation of the data. The phase shifters then only need to switch at the channel innovation rate, which is in the range of a few hundred Hz to the low kHz for a 60GHz system.[3] If the data rate is 1Gbps it is evident that the phase shifters will appear to be static over long intervals.

V. A BEAMFORMING RF FRONT-END

An adaptive antenna array consists of a set of antennas, usually all of the same type, and usually arranged in some regular pattern. Each antenna is excited by the same signal, but this signal is weighted independently for each antenna. This is shown conceptually in Figure 2. [2]

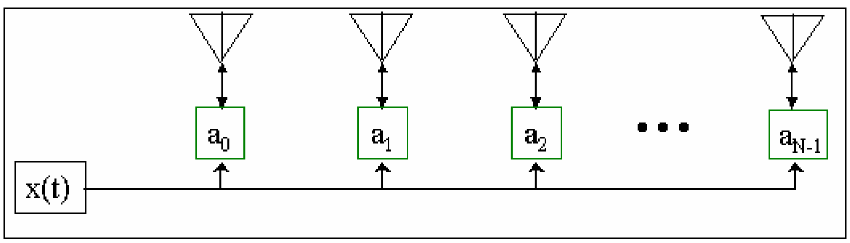

Figure 2. Conceptual Diagram of Adaptive Antenna Array

Furthermore, if the antennas are in a straight line, and they have uniform spacing and uniform excitation amplitudes, the array is called a uniform array. Then the weighting factors, [a_i], are simply phase shifts, and the problem of pointing the antenna's beam is reduced to setting the relative phase shifts of the antennas of the array. Throughout the remained of this paper N will refer to the number of antennas in the array.

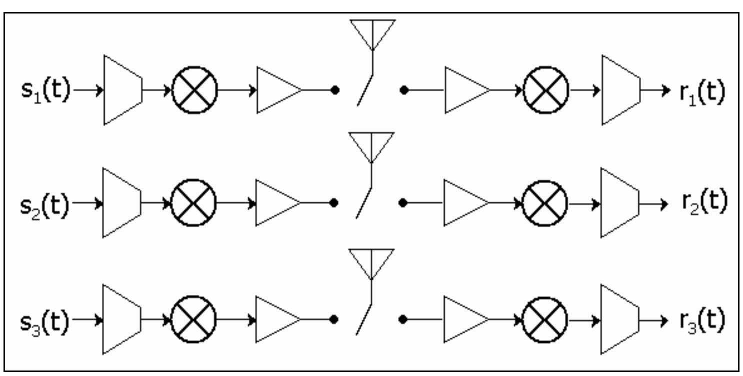

Figure3. Antenna array with a full transceiver for each antenna

There are several ways to build an RF Front-End (RFE) to drive an adaptive antenna array. The core problem is duplicating one master signal to many antennas, while adding phase shifts. The most straightforward way would be to have a full transceiver connected to each antenna. Phase shifts are applied digitally at baseband and each antenna has its own ADC, DAC, PA, LNA[1], mixer and so on. This arrangement is shown in Figure 3 [6]. It has the further advantage that the signal from each antenna can be manipulated and digitized totally independently of the other signals, which allows for MIMO processing. The main drawback of this system is the fact that there are N times as many ADCs, DACs, mixers and so on, as compared to a simple one-antenna system. This could quickly cause the power consumption and die area of the system to become unacceptable. Furthermore, since the 60GHz channel does not typically provide the multipath richness necessary for effective MIMO communications [5], this topology may be overkill.

Our system only needs to apply a phase shift to each antenna independently, and this can be accomplished in a simpler way than that presented above. The phase shifts can be applied in the analog domain. In this arrangement there is only one digital stream, one DAC, and one ADC, but there remain N RF mixers. This way the chip area and power of N-1 ADCs and DACs is saved. This is shown in Figure 4. Note that the mixers are shown as direct-conversion, but this is not necessary. The phase shifts could be applied at IF as well. Also, the mixers and baseband or IF phase shifters need not be separate components. The phase shifts could be applied through variation of the mixers themselves. This architecture better matches the requirements of adaptive beamforming, without the complexity of the previous scheme. A further advantage of this architecture is that it avoids the use of phase shifters at the full carrier frequency, which can be problematic. [7]

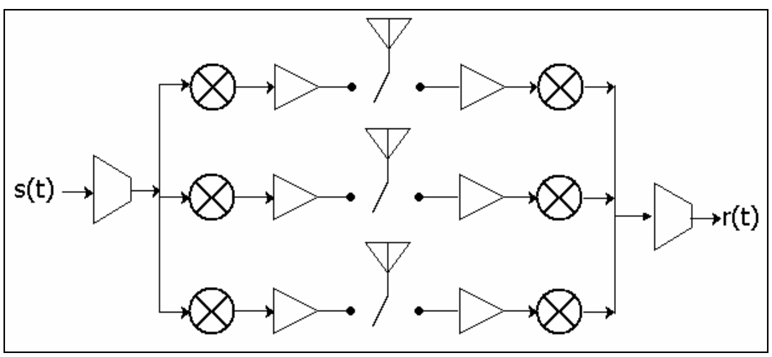

Figure 4. Applying phase shifts at baseband, in analog domain

CMOS circuits operating at 60 GHz are quite difficult to implement, and there is precious little margin to trade between power consumption and outright performance. Therefore, it may not be desirable or even acceptable to have N RF mixers. If it is possible to use only one RF mixer there may be significant savings in power. However, this means that the phase shifting must be performed at the full carrier frequency before combining, which could be difficult. Recalling that the phase selection accuracy only needs to be 3 bits, and that the phase only needs to be adapted at the channel innovation

[1] ADC: Analog to Digital Converter, DAC: Digital to Analog Converter, LNA: Low-Noise Amplifier, PA: Power Amplifier

rate, it begins to look as if an RF phase shifter may be advantageous. A beamforming RFE with RF phase shifters is shown in Figure 5. As will be seen in the next section, the RF phase shifters are not only feasible, but also practical.

A system using RF phase shifters has the advantage that there is only one DAC, one RF up-mixer, one RF down-mixer and one ADC. It also retains the advantages of having N PAs and N LNAs. It is important to note that the phase shifters are before the PAs in the transmitter, and after the LNAs in the receiver. This means that the phase shifters in the transmitter do not need to handle high input power, nor do they need to achieve significant power gain. The situation is similar in the receiver. The phase shifters will operate on a signal that has already been amplified. The phase shifters need not significantly amplify the signal, and the addition of noise should be less critical since they will already enjoy a healthy input signal level. The performance constraints on the RF phase shifters are far lower than what would be required for RF mixers. Most importantly the switching frequency goes from the full carrier frequency of 60GHz for an RF mixer, to the channel innovation rate of a few hundred Hz or less for the RF phase shifters. Therefore, if the phase shifters are properly designed, the use of RF phase shifters should give all the benefits of adaptive antenna arrays, with the minimum added power.

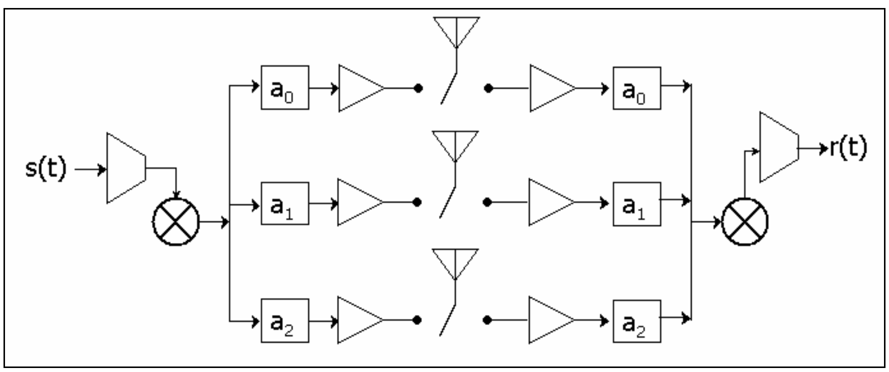

Figure 5. Beamforming RFE with RF phase shifters.

The digital computational advantage of CMOS will come to bear on the antenna array through the control and calibration of the array through the adaptation of the weighting factors. Systematic errors in the array must be learned and compensated for digitally. Most notably, the different path lengths from the active circuits on-chip to the antennas will cause undesired phase shifts which in turn will have a marked effect on the overall antenna pattern.

VI. PHASE SHIFTERS TYPE SELECTION

There are several distinct classes of phase shifters that are typically used. The first is a passive tuned network. This takes the form of an all-pass network that includes some tunable elements. Variation of these elements can change the delay through the network. This type has the disadvantage that it has a limited range of phase shifts that it can perform [8]. This type was used in the past when beams only needed to be steered over a small area, and hence phase shifters only needed a limited range.

Another type is the switched delay-line [9]. This type operates by introducing actual time delays into the signal path. This has the advantage of being wideband, since time delays are frequency independent, whereas phase shifts are the result of mapping a time delay onto a periodic sinusoidal wave. The chief drawback to this approach in a highly-integrated system is that the delay lines can take up a significant amount of area on the chip. The delay lines will be on the order of 0.25 - 1mm long, and will require ample spacing in order to reduce coupling. Recalling that the system may require as many as 16 antennas, it quickly becomes apparent that if we can find another way to implement the phase shifters that takes less area there will be significant savings.

Due to the low accuracy requirements placed on the phase shifters, it is possible to use a vector modulator as a phase shifter. Many communications systems today use some sort of image-rejection mixer that has both an in-phase and quadrature component. A vector modulator phase shifter can be built by simply inserting attenuators into the signal paths of the I and Q channels. For our application, we would first need to split the I and Q signals N-ways and then insert the attenuators, and then recombine the pair of signals before driving the power amplifiers. A vector modulator-type phase shifter is shown schematically in Figure 6 [3].

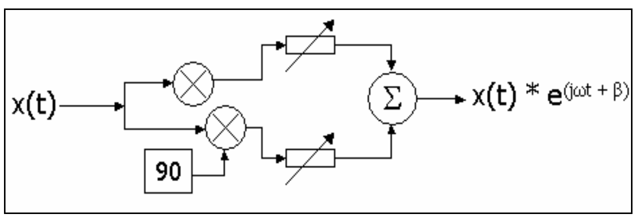

Figure 6. Vector modulator phase shifter

The key to this architecture is not only that the accuracy is only 3 bits, but that each I or Q path only requires 1.5 bits of attenuation. This reduces the attenuators to circuits that simply need to pass their input signal, invert their input signal or cancel their input signal completely, which we will call a Pass-Invert-Cancel circuit, or PIC circuit.

VII. PHASE SHIFTER CIRCUITS

The implementation of the phase shifter comes down to design of the PIC circuit. Here again, we have many options. In the interest of saving space and power in the system, it is best to assert that the RF front end be operated differentially. Thus, positive and negative versions of the I and Q signals will be available. Therefore, the PIC circuit need only select from one of these signals.

The first stage of the PIC circuit will need to be an input buffer, and it will need an output buffer. Between the two buffers is the circuit that will actually do the selection. The basic configuration of the PIC circuit is shown in Figure 7. For the pass-gates to have the lowest on-resistance the drain and source nodes should be biased at the same potential, and the gate should be as high as possible above that potential. In other words V_{GS} should be as high as possible, and V_{DS} should be 0. This biasing scheme also means that the pass-gates will consume no static power. The insertion loss through the entire PIC circuit should not be too severe, since the loss in the pass-gates can be compensated by the gain of the buffers. Recall also that the phase shifters are in positions in the signal path where gain is not critical.

IIX. CONCLUSIONS

The 60Ghz band promises to provide a means of achieving very high data rate communications. With its 5-7GHz of bandwidth this band will allow communications in the range of gigabits per second. Of course, the band is not without its challenges. Path loss is more severe and implementing a highly integrated transceiver in CMOS will be challenging at the very least. Many of these drawbacks can be overcome through the use of an adaptive antenna array. The adaptive array introduces a few problems of its own, such as calibration of the phase shifters, but these should be solvable. In the end, it should be possible very soon for the 60GHz band to be utilized to its full potential.

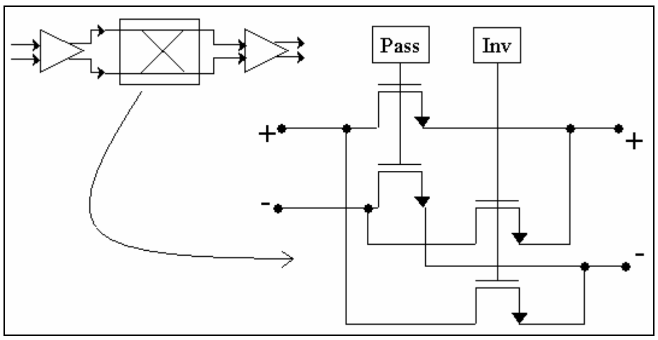

Figure 7. PIC circuit block diagram and core

REFERENCES

[1] C. A. Balanis, Antenna Theory, Analysis and Design, 2nd ed., John Wiley and Sons, New York, 1997
[2] R. C. Hansen, Phased Array Antennas, John Wiley and Sons, New York, 1998
[3] J. G. Proakis, Digital Communications, McGraw-Hill, San Francisco, 1995
[4] S. Ramo, J. Whinnery, T. Van Duzer, Fields and Waves in Communications Electronics, 3rd ed., John Wiley and Sons, New York, 1994
[5] C. Doan, S. Emami, A. Niknejad, R. Brodersen, "Design of CMOS for 60GHz Applications," *ISSCC Dig. Tech Papers*, pp. 440-441, Feb. 2004
[6] Berkeley Wireless Research Center Website, http://bwrc.eecs.berkeley.edu
[7] H. Hashemi, X. Guan, A. Hajimiri, "A Fully Integrated 24GHz 8-Path Phased-Array Receiver in Silicon," *ISSCC Dig. Tech Papers*, pp. 390-391, Feb. 2004
[8] F. Ellinger et. al., "Ultra-Compact Reflective-Type Phase Shifter MMIC at C-Band with 360° Phase-Control Range for Smart-Antenna Combining," *IEEE J. Solid-State Circuits*, vol. 37, pp.481-486, Apr. 2002
[9] D. M Pozar, Microwave Engineering, 2nd ed., John Wiley and Sons, New York, 1998